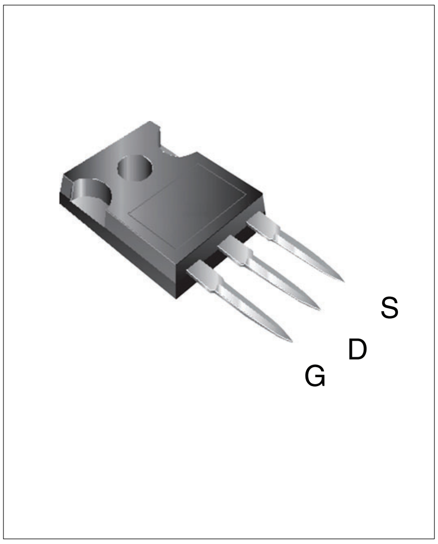
40Amps, 100Volts
N-CHANNEL POWER MOSFET



*Pb-free plating product number: IRF150

■ DESCRIPTION

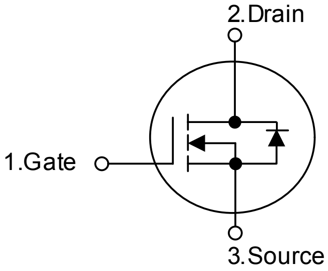
The YR IRF150 is three-terminal silicon device with current conduction capability of about 40A, fast switching speed. Low on-state resistance, breakdown voltage rating of 100V, and max threshold voltages of 4 volt.

It is mainly suitable electronic ballast, and low power switching mode power appliances.

■ FEATURES

* $R_{DS(ON)}$ = 15mΩ@V_{GS} = 10 V
* Ultra low gate charge (typical 670 nC)
* Low reverse transfer Capacitance (C_{RSS} = typical 78 pF)
* Fast switching capability
* 100% avalanche energy specified
* Improved dv/dt capability

■ SYMBOL



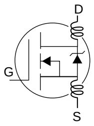
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	40	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	25	
I_{DM}	Pulsed Drain Current ①	160	
P_D @T_C = 25°C	Power Dissipation	150	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current①	19	A
E_{As}	Repetitive Avalanche Energy①	150	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.8	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

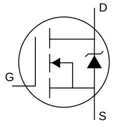
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.80	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	30	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.13	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	15	m Ω	V_{GS} = 10V, I_D =20A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance35		——	——	S	V_{DS} = 25V, I_D = 20A④
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	μA	V_{DS} = 100V, V_{GS} = 0V
		——	——	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	——	120I	CV	$_D$ = 20A
Q_{gs}	Gate-to-Source Charge	——	——	25 n		$_{DS}$ = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	40V		$_{GS}$ = 10V, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	——	13	——	ns	V_{DD} = 50V
t_r	Rise Time	——	55	——		I_D = 20A
$t_{d(off)}$	Turn-Off Delay Time	——	43	——		R_G = 2.5Ω
t_f	Fall Time	——	45	——		V_{GS} = 10V, See Fig. 10 ④
L_D	Internal Drain Inductance	——	4.2	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	——	7.2	——		
C_{iss}	Input Capacitance	——	2980	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	400	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	78	——		ƒ = 1.0MHz, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy②	——	1060⑤	280⑥	mJ	I_{AS} = 20A, L = 0.70mH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	40	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)①	——	——	160		
V_{SD}	Diode Forward Voltage	——	——	1.2	V	$T_J = 25°C$, $I_S = 20A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	——	140	220	ns	$T_J = 25°C$, $I_F = 20A$ di/dt = 100A/µs ④
Q_{rr}	Reverse Recovery Charge	——	670	1010	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25°C$, L = 0.70mH $R_G = 25\Omega$, $I_{AS} = 20A$, V_{GS}=10V (See Figure 12)

③ $I_{SD} \le 20A$, di/dt ≤ 380A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le 175°C$

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to $T_J = 175°C$.

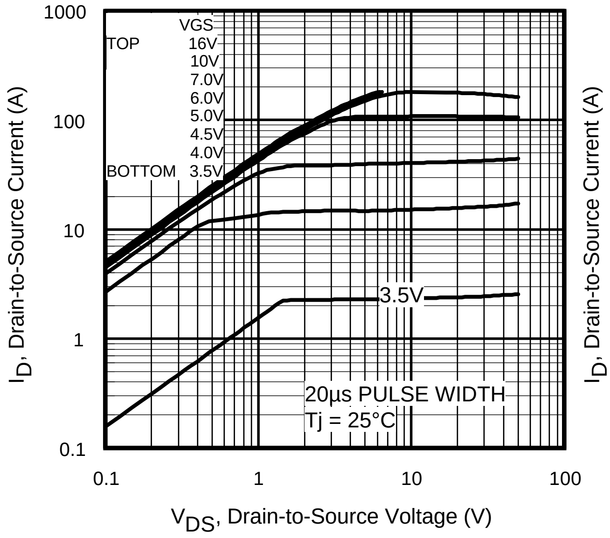


Fig 1. Typical Output Characteristics

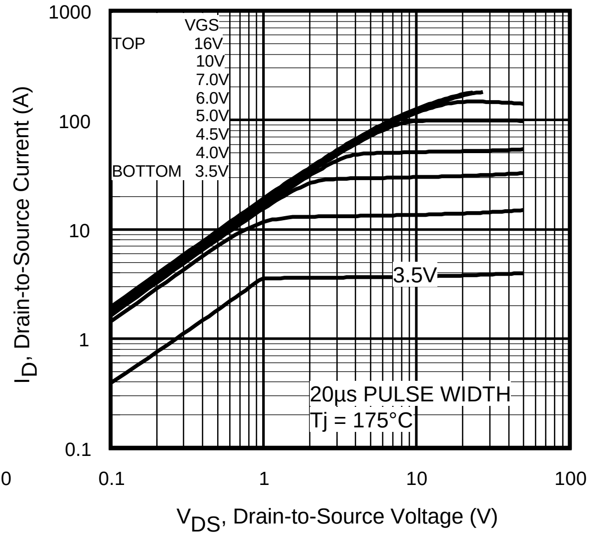


Fig 2. Typical Output Characteristics

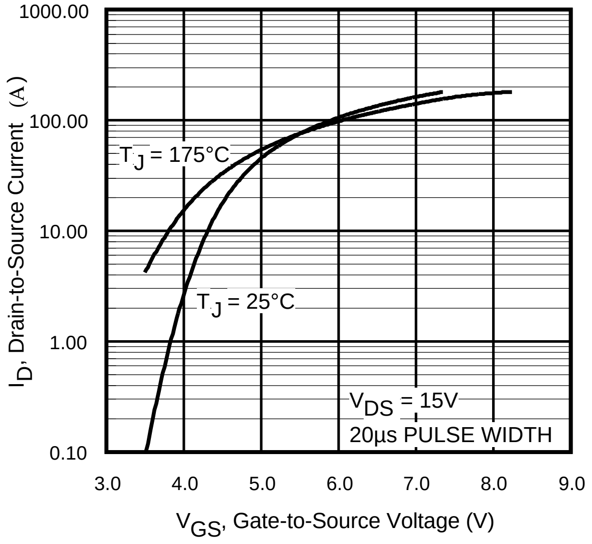


Fig 3. Typical Transfer Characteristics

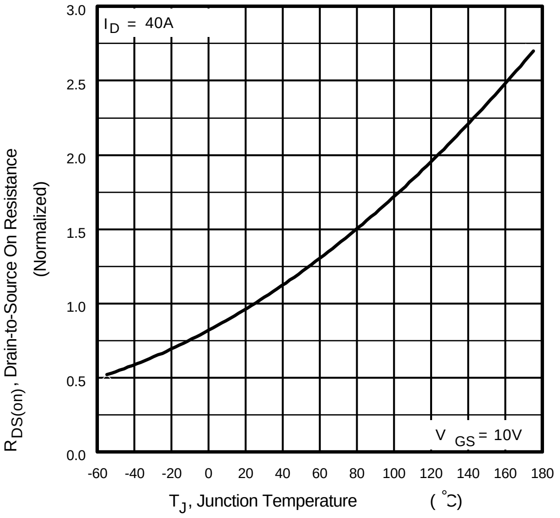


Fig 4. Normalized On-Resistance Vs. Temperature

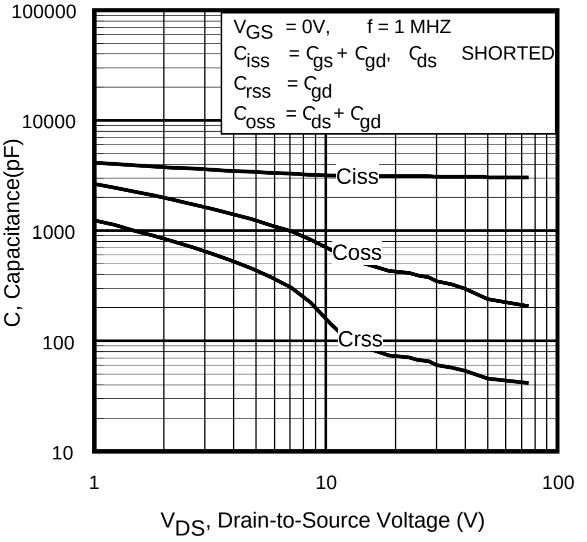


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

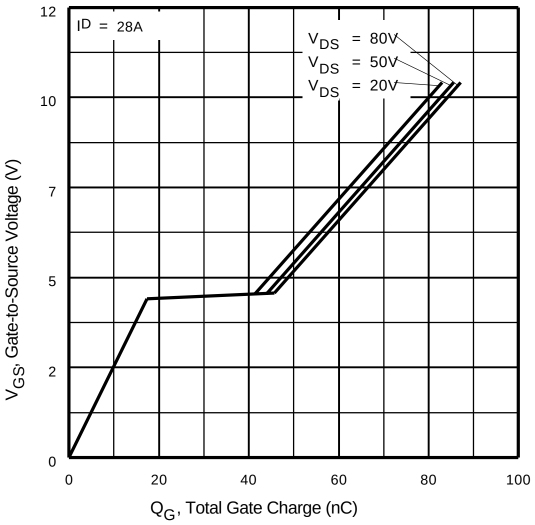


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

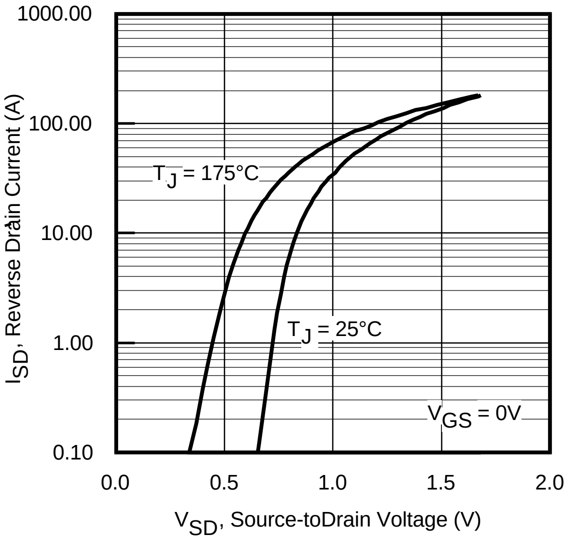


Fig 7. Typical Source-Drain Diode

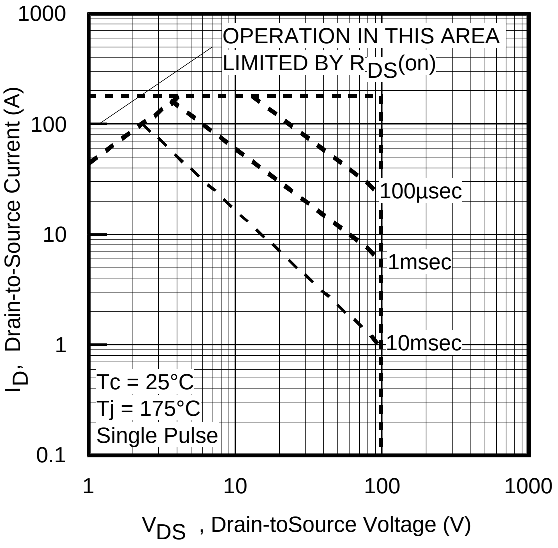


Fig 8. Maximum Safe Operating Area

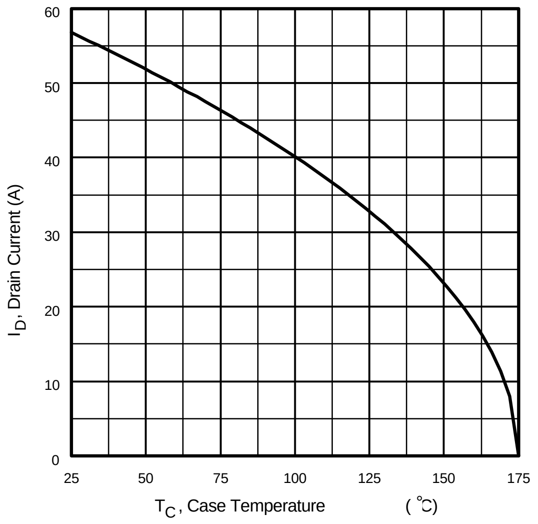


Fig 9. Maximum Drain Current Vs. Case Temperature

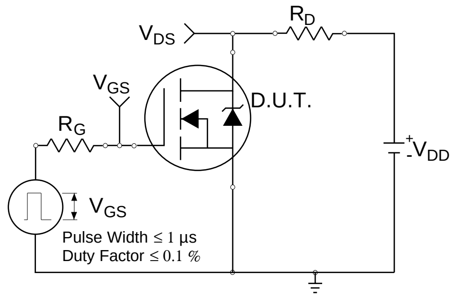


Fig 10a. Switching Time Test Circuit

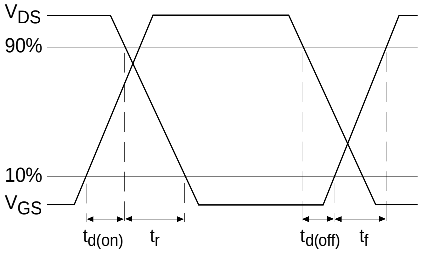


Fig 10b. Switching Time Waveforms

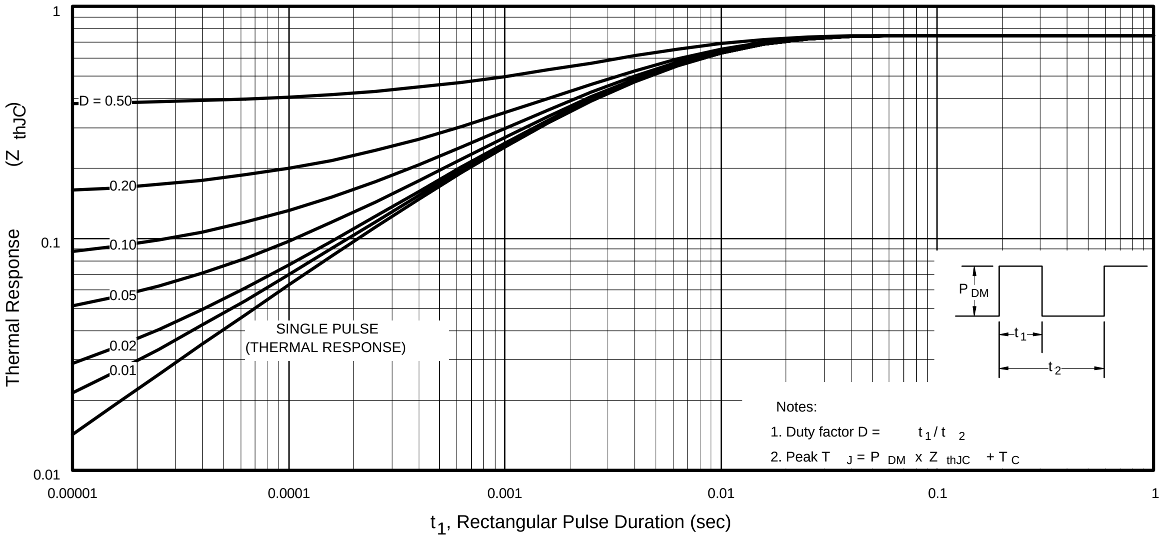


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

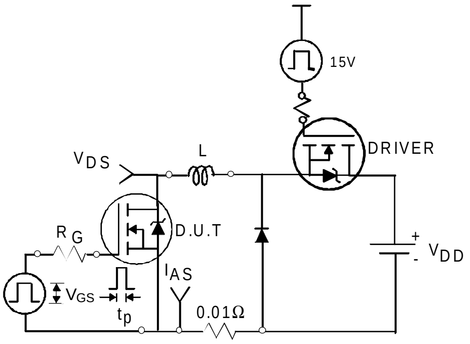


Fig 12a. Unclamped Inductive Test Circuit

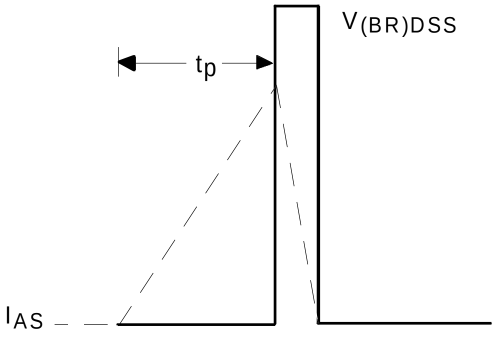


Fig 12b. Unclamped Inductive Waveforms

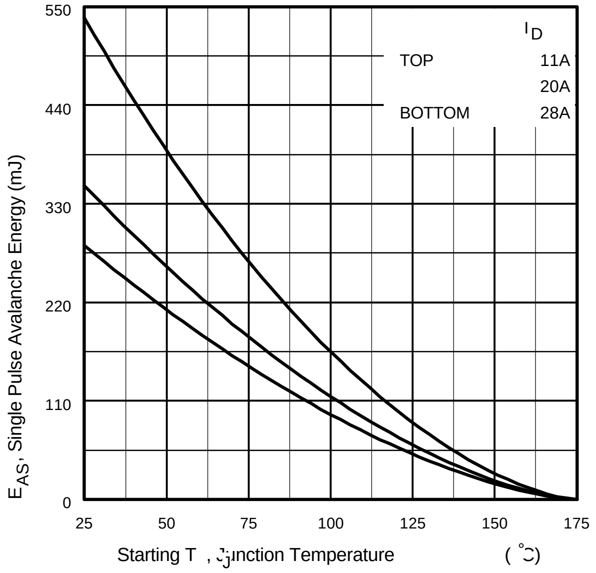


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

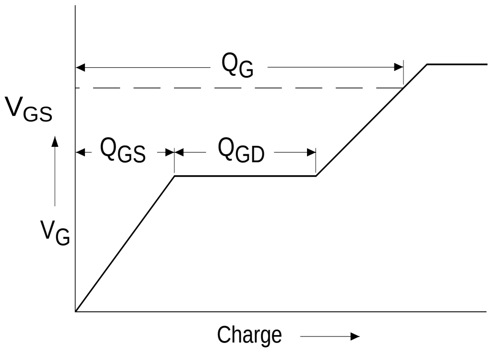


Fig 13a. Basic Gate Charge Waveform

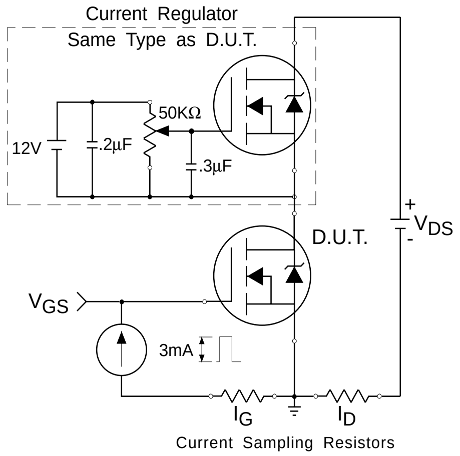
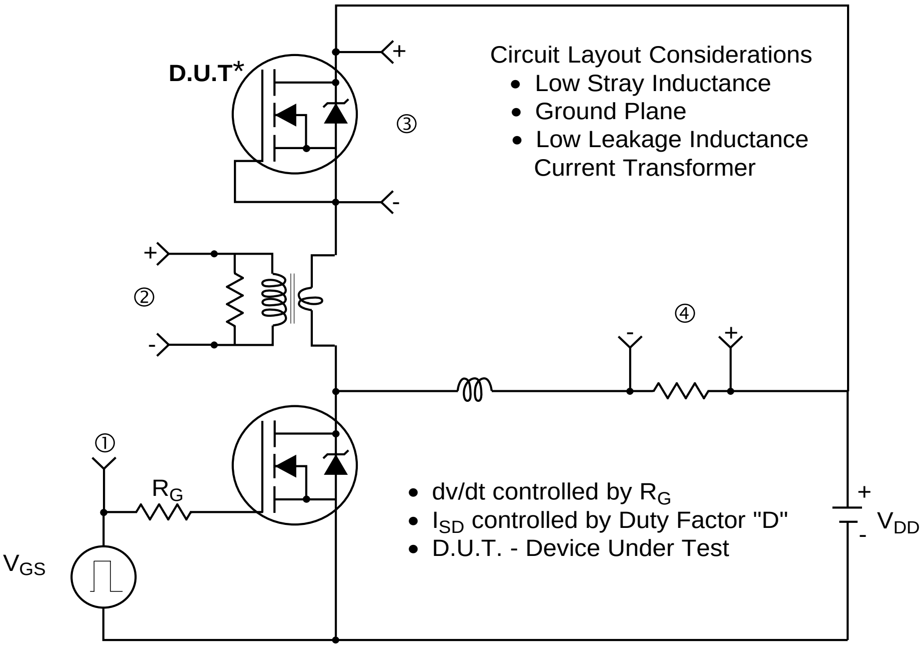
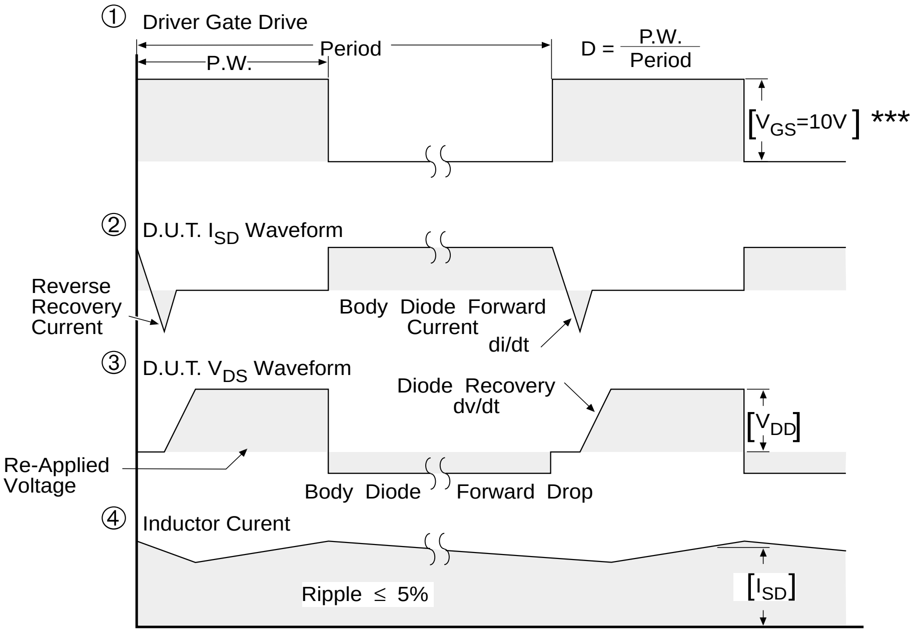


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs