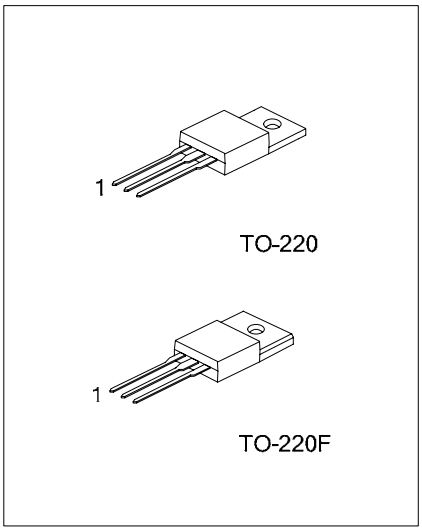
YAREN TECHNOLOGY

6N60

Power MOSFET

5.5 Amps, 600 Volts
N-CHANNEL MOSFET



*Pb-free plating product number: 6N60

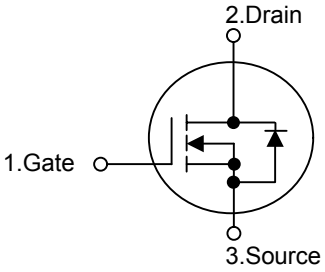
■ DESCRIPTION

The YR6N60 is a high voltage MOSFET and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in switching power supplies and adaptors.

■ FEATURES

* $R_{DS(ON)}$ = 2.0Ω @V_{GS} = 10V
* Ultra low gate charge (typical 20 nC)
* Low reverse transfer Capacitance (C_{RSS} = typical 10pF)
* Fast switching capability
* Avalanche energy tested
* Improved dv/dt capability, high ruggedness

■ SYMBOL



■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage	6N60	V_{DSS}	600	V
	6N65		650	V
Gate-Source Voltage		V_{GSS}	±20	V
Avalanche Current (Note 1)		I_{AR}	5.5	A
Continuous Drain Current	T_C = 25°C	I_D	5.5	A
	T_C = 100°C		3.0	A
Pulsed Drain Current (Note 1)		I_{DM}	24.8	A
Avalanche Energy	Single Pulsed (Note 2)	E_{AS}	440	mJ
	Repetitive (Note 1)	E_{AR}	13	mJ
Power Dissipation		P_D	62.5	W
Junction Temperature		T_J	+150	℃
Operating Temperature		T_{OPR}	-55 ~ +150	℃
Storage Temperature		T_{STG}	-55 ~ +150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction-to-Ambient	θ_{JA}	62	°C/W
Junction-to-Case	θ_{JC}	2	°C/W

■ ELECTRICAL CHARACTERISTICS (T_J =25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	6N60	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	600			V
	6N65			650			V
Drain-Source Leakage Current		I_{DSS}	V_{DS} = 600V, V_{GS} = 0V			10	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS} = 20V, V_{DS} = 0V			100	nA
	Reverse		V_{GS} = -20V, V_{DS} = 0V			-100	nA
Breakdown Voltage Temperature Coefficient		$\triangle BV_{DSS}/\triangle T_J$	I_D = 250 μA, Referenced to 25°C		0.53		V/℃
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS} = 10V, I_D = 2.75A		1.7	2.0	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C_{ISS}	V_{DS}=25V, V_{GS}=0V, f=1.0 MHz		770	1000	pF
Output Capacitance		C_{OSS}			95	120	pF
Reverse Transfer Capacitance		C_{RSS}			10	13	pF
SWITCHING CHARACTERISTICS							
Turn-On Delay Time		$t_{D(ON)}$	V_{DD}=300V, I_D =5.5A, R_G =25Ω (Note 4, 5)		20	50	ns
Turn-On Rise Time		t_R			70	150	ns
Turn-Off Delay Time		$t_{D(OFF)}$			40	90	ns
Turn-Off Fall Time		t_F			45	100	ns
Total Gate Charge		Q_G	V_{DS}=480V, I_D=5.5A, V_{GS}=10 V (Note 4, 5)		20	25	nC
Gate-Source Charge		Q_{GS}			4.9		nC
Gate-Drain Charge		Q_{GD}			9.4		nC

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 5.5 A			1.4	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				5.5	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				24.8	A
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 6.0 A,		290		ns
Reverse Recovery Charge	Q_{RR}	dI_F/dt = 100 A/μs (Note 4)		2.35		μC

Notes: 1. Repetitive Rating : Pulse width limited by T_J

2. L = 16.8mH, I_{AS} = 5.5A, V_{DD} = 90V, R_G = 25 Ω, Starting T_J = 25°C

3. I_{SD} ≤ 5.5A, di/dt ≤200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

4. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%

5. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

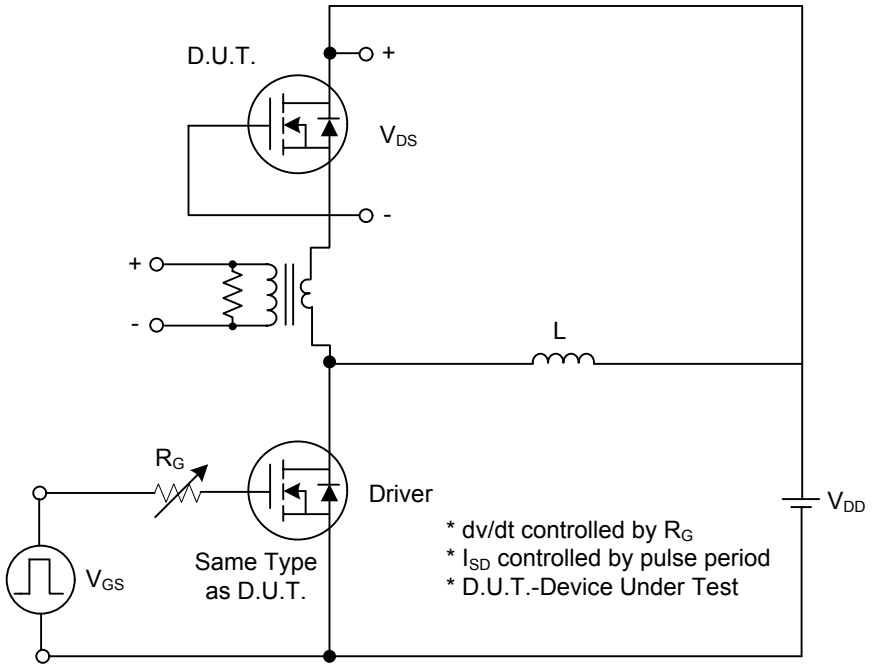


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

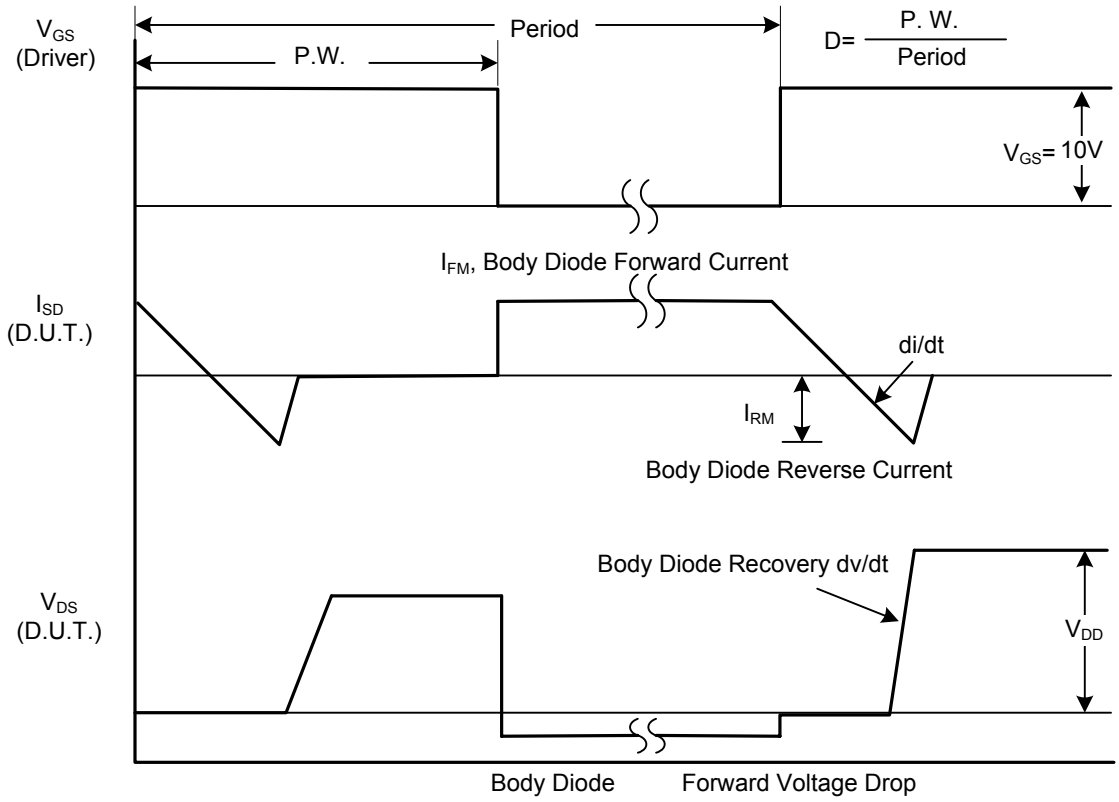


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

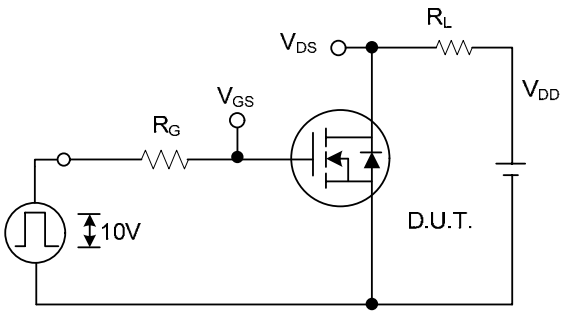


Fig. 2A Switching Test Circuit

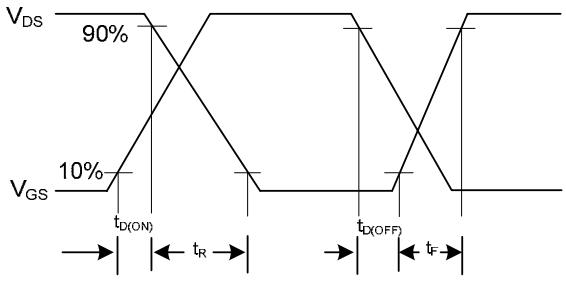


Fig. 2B Switching Waveforms

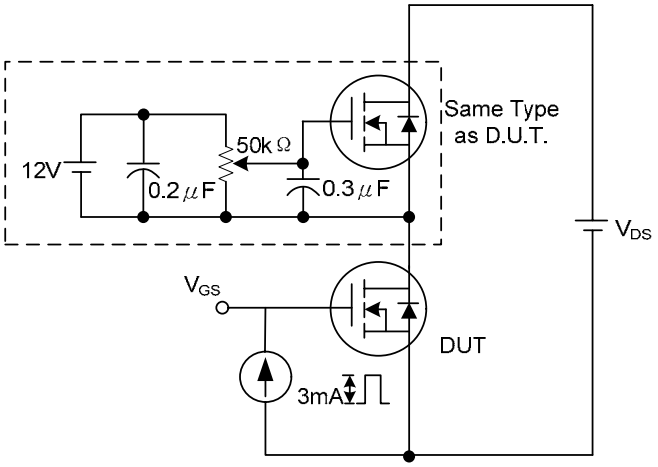


Fig. 3A Gate Charge Test Circuit

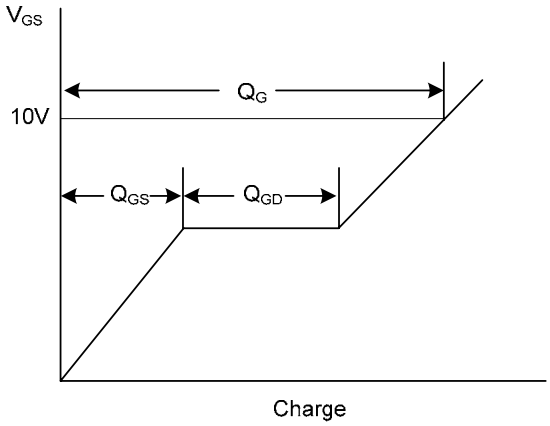


Fig. 3B Gate Charge Waveform

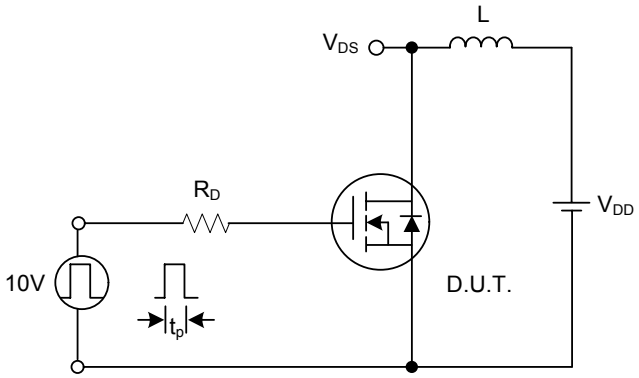


Fig. 4A Unclamped Inductive Switching Test Circuit

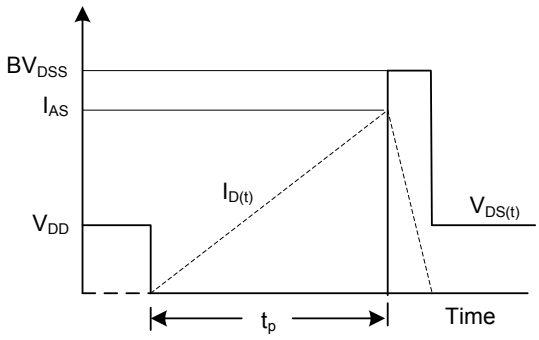


Fig. 4B Unclamped Inductive Switching Waveforms